Docket No.: 1190-0618PUS1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Tomoaki RYU

Application No.: 10/566,728

Confirmation No.: 9704

Filed: February 2, 2006

Art Unit: 4148

For: DIGITAL RECORDING APPARATUS, DIGITAL REPRODUCING APPARATUS, DIGITAL RECORDING/REPRODUCING APPARATUS, ENCRYPTION APPARATUS, DECRYPTION APPARATUS, ENCRYPTION METHOD, AND DECRYPTION METHOD

Examiner: T. D. Pogmore

REQUEST FOR PRE-APPEAL BRIEF CONFERENCE

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

INTRODUCTORY COMMENTS

Applicant requests review of the Final Rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed concurrently with a Notice of Appeal.

The review is being requested for the reasons set forth on the attached sheets.

ARGUMENTS

The Examiner Has Failed To Establish *Prima Facie* Obviousness By Failing To Provide References that Teach or Suggest All Of The Claim Elements

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hashimoto (U.S. Patent No. 4,907,275) in view of Hasebe et al. (U.S. Patent No. 5,392,351, hereinafter "Hasebe") in further view of Yokota et al. (U.S. Patent No. 7,230,898, hereinafter "Yokota"). Also, claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hashimoto in view of Hasebe.

For a 35 U.S.C. § 103 rejection to be proper, a prima facie case of obviousness must be established. See M.P.E.P. 2142. One requirement to establish prima facie case of obviousness is that the prior art references, when combined, must teach or suggest all claim limitations. See M.P.E.P. 2142; M.P.E.P. 706.02(j). Thus, if the cited references fail to teach or suggest one or more elements, then the rejection is improper and must be withdrawn.

Independent claim 1 recites, *inter alia*, "when the digital recording signal needs to be encrypted, the encryption circuit begins to start up and the digital recording signal is transmitted from the data control circuit to the memory to be stored in the memory **during start-up of the encryption circuit**, and when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in the recording unit." It is respectfully submitted that the cited references fail to teach the above-identified claim elements.

Hashimoto describes an encryption apparatus including an input buffer 14, an encryption processor 15 and an output buffer 16. A plain text block sequence is input into input buffer 14. The encryption processor 15 encrypts the plain text block sequence one block at a time and stores it into the output buffer 16. The plain text blocks not to be encrypted are sequentially read from the input buffer in the ascending order of the addresses and they are stored, without being encrypted, in the output buffer at the corresponding addresses to the input buffer addresses at which the plain text blocks have been stored. See Abstract, lines 1-15 of column 3 and Figure 2B of Hashimoto. In other words, Hashimoto is directed to utilizing an input buffer to ensure a sequential process of encrypting the stored data.

However, Hashimoto does not disclose or suggest that when a digital recording signal needs to be encrypted, an encryption circuit begins to start up and the digital recording signal is transmitted from a data control circuit to a memory to be stored in the memory during start-up of the encryption circuit as claimed. Also, Hashimoto fails to disclose or suggest that when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in a recording unit as claimed.

The Examiner asserts that Hashimoto, in lines 1-15, col. 3, discloses or suggests the above-identified claimed features. Contrary to the assertion by the Examiner, the cited portion of Hashimoto merely describes an input buffer 14 to store a plain text block sequence. The encryption processor 15 encrypts the plain text block sequence one block at a time and stores it into the output buffer 16. However, Hashimoto is completely silent with respect to the process of a digital recording/reproduction signal **during the time period when an encryption/decryption circuit is starting up [enabling]**.

In responding to Applicant's above-mentioned arguments, the Examiner alleges that the inherent property of a buffer is to temporarily store data for whatever reason. In addition, the Examiner admits that Hashimoto does not teach processing a digital recording/reproduction signal **during the time period when an encryption/decryption circuit is starting up [enabling]**. However, the Examiner erroneously concludes that the lack of teaching by Hashimoto is irrelevant because the intended use of a buffer is to store data after it is transferred but before it can be processed either due to the circuit not having completed start-up or is currently processing other data. Such allegation is simply without merit and unsupported.

First, the mere disclosure of a buffer does not remedy the deficiency of Hashimoto with respect to processing of a digital recording/reproduction signal **during the time period when an encryption/decryption circuit is starting up [enabling]** as claimed.

Furthermore, the mere disclosure of an input buffer does not provide any support for an assertion that Hashimoto discloses a buffer for storing data before it can be processed due to the circuit not having completed start-up. Hashimoto is not concerned with respect to a buffer for the alleged purpose. In contrast, Hashimoto discloses an input buffer for the purpose of encrypting

the data one block at a time to ensure a sequential processing. See lines 1-15, col. 3 of Hashimoto. Thus, it would not have been obvious to one of ordinary skill in the art at the time of invention to modify Hashimoto to use the buffer for the purpose of storing data before it can be processed due to the circuit not having completed start-up. The Examiner appears to mischaracterize Hashimoto in an effort to satisfy the claimed features.

Even assuming, *arguendo*, that the inherent property of a buffer is to temporarily store data for whatever reason as alleged, the combination of the buffer and Hashimoto still does not teach or suggest "wherein when the digital recording signal needs to be encrypted, the encryption circuit begins to start up and the digital recording signal is transmitted from the data control circuit to the memory to be stored in the memory during start-up of the encryption circuit, and when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in the recording unit" as claimed. Specifically, Hashimoto is completely silent with respect to starting up the encryption circuit when the digital recording signal needs to be encrypted and processing the digital recording data during start-up of the encryption circuit. A buffer with the alleged inherent property of temporarily storing data for whatever reason does not make up for the above-noted deficiency of Hashimoto.

In addition, with the arrangement of claimed features, a recording/reproducing unit enables an encryption/decryption circuit only when encryption/decryption is required without interrupting recording/reproducing. As such, data can be continuously recorded/reproduced during a period of time from a time when a program that does not need to be encrypted/decrypted is switched to a program that needs to be encrypted/decrypted to a time when the recording/reproducing unit is ready to record/reproduce an encrypted/decrypted signal. As a result, a digital signal can be recorded or reproduced during start-up of an encryption circuit or decryption circuit.

Hashimoto is not concerned with providing such features. Thus, the Examiner's reasoning for supporting the allegation appears to be based on impermissible hindsight. See MPEP 2141. Hasebe and Yokota do not remedy the deficiencies of Hashimoto.

In view of the above remarks with respect to independent claim 1, Applicant respectfully submits that the grounds of rejection fails to establish that the prior art teaches enabling an encryption/decryption circuit when encryption/decryption is required and processing a digital recording/reproduction signal during the time period when the encryption/decryption circuit is starting up [enabling] as claimed. Independent claims 2, 4, 7, 10 and 11 recite similar features and are also distinguishable from the applied art for the reasons discussed with respect to claim 1. Consequently, the rejection fails to establish prima facie obviousness of any of the rejected claims. Thus, Applicant respectfully requests reconsideration withdrawal of the Examiner's rejection under 35 USC § 103.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Dennis P. Chen, Reg. No. 61,767, at (703) 205-8000, to schedule an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: August 5, 2009

Respectfully submitted,

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